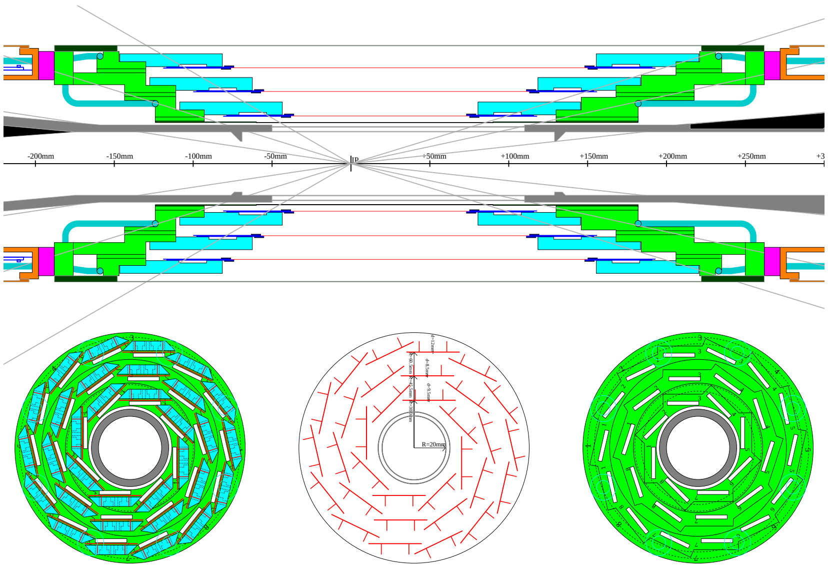

Figure 1: Detector configuration

Here, the DSSD fabricated by Hamamatsu Photonics (HPK) originally designed for the DELPHI micro vertex detector [2] is used. The DSSDs will be wire bonded to front end VLSI chips. The performance to carry our physics objectives, in particular, the first observation in CP asymmetry in $J/\Psi K_s$ decay mode will be described in the next section.

The key item that defines our readout electronics is the front end VLSI chip. By choosing it, almost entire readout chain is defined. We have chosen the VA1 chip, which is developed at CERN and is commercially available from IDE AS, Oslo, Norway. The DSSDs are wire bonded to VA1 chips mounted on the hybrid boards. The VA1 chip is produced in 1.2 μm CMOS technology. It contains 128 low power (1.2 mW/channel) charge sensitive preamplifiers followed by CR-RC shapers and sample & hold circuitry, output multiplexing and one output buffer. The output channels are daisy chained, and read out at 5 MHz (which needs to be verified). At BELLE we operate VA1 chip with a peaking time of 2.5μsec due to the trigger latency. With this peaking time we expect the noise performance will be about $(165 + 6.1 \times C)$ electrons equivalent noise charge, where C is the capacitance at the input in pF, giving less than 400 electrons for 35 pF, the average strip capacitance expected. We have experience using VA1 chips with DSSDs including our own prototype sensors and we are confident that the required signal to noise ratio will be achieved with VA1 chips. There exist some information on radiation-hardness of the VA1 chip. It's prototype indicated that it could stand up to 200 krad[3]. IDE AS also provides the radiation hard version of VA1 chip (RH1) whose initial noise performance, $375 + 8.6 \times C$ electrons, is worse than VA1. It may, however, surpass VA1 after some irradiation. We plan to study the noise figures for VA1 and RH1 as a function